A 2.5-Watt High Efficiency X-Band Power MMIC

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Abstract

The design and performance of a 2-stage MBE monolithic power amplifier chip are presented. The MBE monolithic chip contains full interstage matching, partial matching at the input, and no match at the output. When matched to 50 ohms at input and output using off-chip circuitry, the MMIC demonstrated best overall performance of 34dBm (0.436W/mm), 36%, and 14.5dB of power, power-added-efficiency (PAE), and associated gain respectively, across the band of 9.0-10.0 GHz. The PAE was as high as 38% in parts of the band. The average performance considering 26 devices from at least 12 wafers from 5 different runs was 33.6dBm (.4W/mm), 32%, and 14dB, respectively. The chip size was very compact at 0.081"x0.070"x0.003" (2.06x1.78 mm^2).

Introduction

The need for high power density, high efficiency and small physical size for power stages is self evident when targeting applications such as Transmit/Receive modules. The need for low cost is even more obvious considering the large volumes involved per phased array radar. The solution to satisfy all the above requirements simultaneously is not available at present. A complete monolithic implementation of such a power block by numerous organizations has not proven realistic up to the present time [1],[2]. A plausible solution advanced here is that of partial monolithic implementation of a 2-stage X-band power amplifier. The 2-stage MMIC has on-chip, full interstage match, partial input match, and no output match. This results in a chip size that is drastically reduced with all the obvious attendant advantages; The critical output circuit losses are off-chip and so are well controlled, and off-chip tuning is provided for, if needed, to optimize the performance of the individual amplifiers. Further, due to the smaller die size, chip handling is easier and die attach is more reliably controlled. The partial input match presents a reasonable level of input impedance to the off-chip input circuitry. The level of impedances at both input and output of the MMIC permits the off-chip circuitry to be relatively simple and the assembly, non critical. All this prevents significant escalation in cost without compromising performance, with only a slight penalty for some extra non critical assembly. Given the product specification, the design approach was: use a proven high efficiency device; use a thinner chip for better heat dissipation; control the circuit losses in the interstage and output circuits; minimize the die size as much as possible.

Active device details

The MMIC uses a 2.2mm FET driving a 5.76mm FET. The driver FET consists of 4cells x 8 fingers/cell x 68.75 um width/gate fingers. The 5.76 mm FET consists of 8 cells x 8 fingers/cell x 90 um width/gate fingers. The reason for selecting this pattern was to realize 2^n cells for each FET in order to facilitate a symmetric binary tree architecture for the MMIC. The vertical FET geometry is identical to the high performance MBE HI-LO-HI device described earlier [1]. The nominal gate length is 0.4um. The pitches used are 18.5um for the driver and 20.5um for the output FETs respectively. A unit FET of 1.8mm gate width routinely delivers 29.5dBm (0.5W/mm) with at least 7dB associated gain and greater than 40% power-added-efficiency (PAE) at 10.2 GHz when biased at 9.0V and 20% IDSS.

FET Modeling

Two port small signal s-parameters were measured on several representative 1.8 mm FETs under class-A bias. From these the well known small signal equivalent circuit of the FETs was determined. Experimental broad-band load-pull and source-pull measurements were used to establish 1-port simplified equivalent

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circuit models for the input and output for optimum power and efficiency.

Circuit Design

Figure 1 shows a picture of the MMIC and figure 2 shows the schematic diagram for half the MMIC. The interstage design was the most important part of the MMIC design. The FET model used in the interstage design was solely based on the empirical simplified equivalent circuits discussed above. The small signal s-parameters were used as a final check on the overall design's small signal performance and broad-band stability. No consideration was given to harmonic tuning. The MMIC is physically and electrically symmetric about the center. The interstage circuit topology was influenced heavily by considerations such as biasing, low loss, and circuit realizability in a minimum of space. All series capacitors and shunt inductors provide both biasing and matching functions. The widths of the line feeding the current to the drain of the driver FET were constrained to carry IDSS. The widths of other lines were chosen from circuit design, layout ease, and loss considerations. An earnest attempt was made to minimize junction discontinuities and unintentional coupling between adjacent structures. No attempt was made to "de-Q" the immediate match at the input of the 5.76mm FET. The match between the two FETs was flat and optimized to maximize in-band performance. This approach requires that the input gate capacitance of the FETs be well controlled since the performance is relatively sensitive to changes in FET gate capacitance. A 25 ohm resistor is inserted in the gate bias circuitry for each FET on chip to limit the gate current as well as to provide for added low frequency stability. Odd mode oscillations are inhibited by strapping individual cells of each FET together at both the gate and drain terminals. The input to the MMIC is blocked for DC using on-board MIM capacitors. The complete amplifier with the MMIC and off-chip matching circuitry is shown in figure 3. The off-chip input circuitry is very simple consisting of a single series lumped bond wire inductance and a shunt open stub realized on a .015" thick alumina substrate. The off-chip output match is of a distributed nature and is realized on a .008" thick substrate with Er=38 in order to minimize the size of the circuit. The overall amplifier measures .275"x.130" (excluding extraneous 50 ohm line) and is mounted on a gold plated OFHC copper carrier.

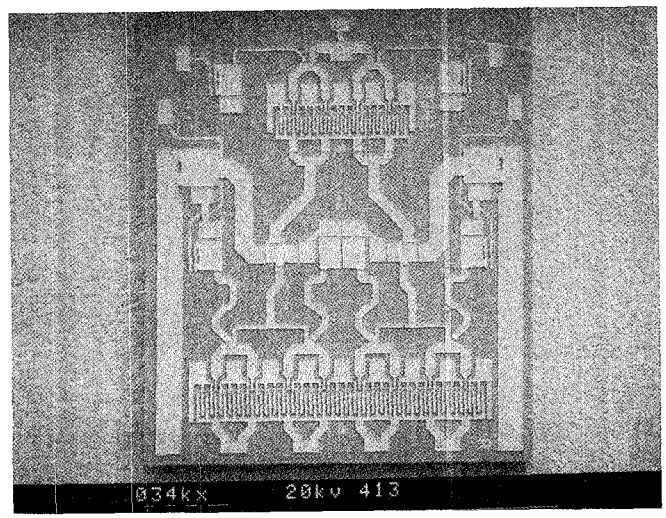
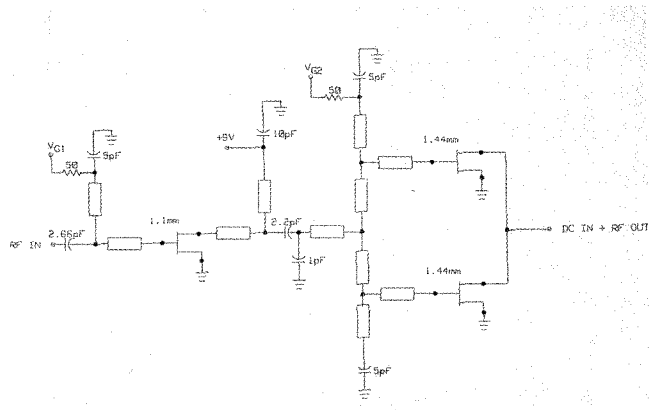


Fig. 1 The M341 MMIC



CIRCUIT SCHEMATIC DIAGRAM OF HALF THE MMIC

Fig. 2 Schematic Diagram for half the MMIC

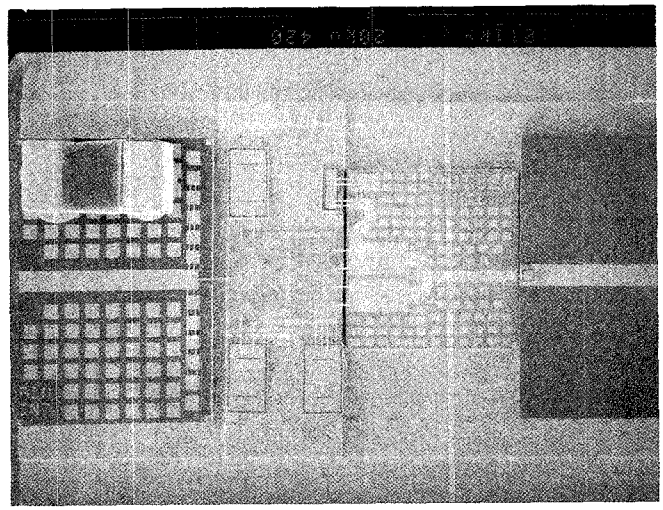


Fig. 3 The Complete Amplifier

MMIC Fabrication

MBE wafers with a special tailored Hi-Lo-Hi profile were used to fabricate the high performance power MMIC's. Material growth and its specifications and the manufacturing process for high performance power FET's has been described elsewhere[3],[4]. A RIE via-hole process was used to ground the source pads as well as the biasing capacitors. Via-holes were defined using the infrared aligner and etched in a reactive ion etcher. The size of the via-holes was minimized for circuit compactness. Next, a thick layer of gold was plated into the holes and over the wafer backside to serve as a plated heat sink. The base metal for the inductor, interconnect, transmission lines and the capacitor bottom plates were realized during gate metallization. Si_3N_4 was used to passivate the active devices and as the dielectric material for the MIM capacitors. An additional overlay metal was used for interconnecting air-bridges, top plates for capacitors, and enhance current handling capability for other elements. GaAs resistors were trimmed during the gate recess and resistor masking step.

RF and Thermal Performance

The MMICs were tested as complete broadband amplifiers assembled as shown in figure 3. The majority of the devices required no tuning except for gate bias optimization. A few wafers required a little tuning of the off-chip bond wire inductances for optimum operation providing clear proof that off chip matching with a few tuning handles can significantly increase the RF yields. Performance of devices within the same wafer were extremely repeatable due probably to the uniformity of the MBE material. Figures 4, 5, and 6 show the performance curves of 26 devices. All data is measured CW at a flange temperature of 30°C and in a broad band 50 ohm system without external tuning of any kind and at the 2-dB gain compression point. The typical quiescent bias was at 30% IDSS at a drain voltage of 9V. The best device with the best overall performance was a power of at least 34dBm (.436W/mm), at least 36% power-added-efficiency, and associated gain of 14.5dB, over the full band of 9.0-10.0 GHz. At several points in the band the efficiency was as high as 38%. The typical consistent performance averaged over 26 devices from 12 wafers from 5 different runs, was a power of 33.6dBm (.4W/mm), efficiency of 32%, and associated gain of 14dB, over the entire band.

Several devices performed adequately over the wider band of 8.8-10.4 GHz with a power of at least 33.5 dBm and a PAE of at least 30%. Figures 7 and 8 show the power and efficiency as a function of input drive level for several frequencies in the band of interest. The observed performance bandwidth correlated quite well with measured 1 MHz gate capacitance measurements on test cells and MMIC die thickness. On MMICs with lower than designed gate capacitance, the performance shifted predictably upward. However, by reducing the quiescent |Vgs| the desired performance bandwidth could be restored in many cases.

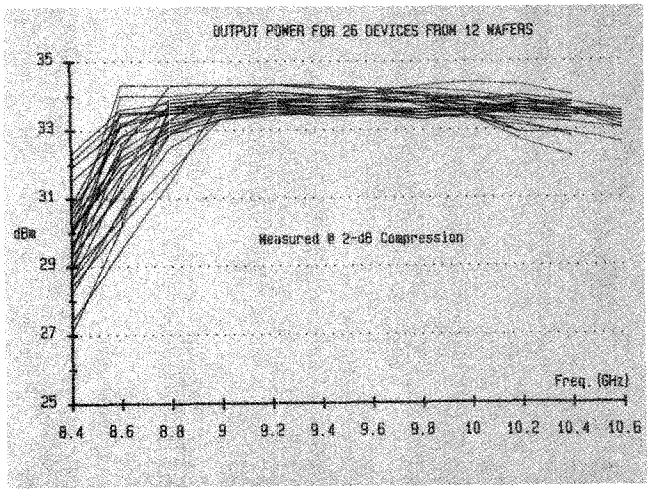


Fig. 4 Output Power for 26 devices

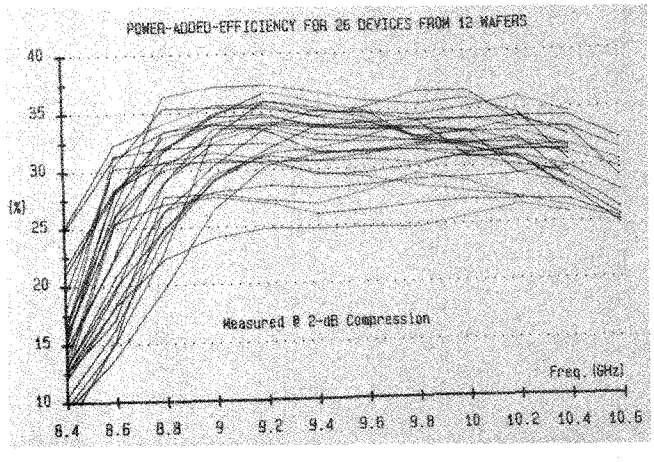


Fig. 5 PAE for 26 devices from 12 Wafers

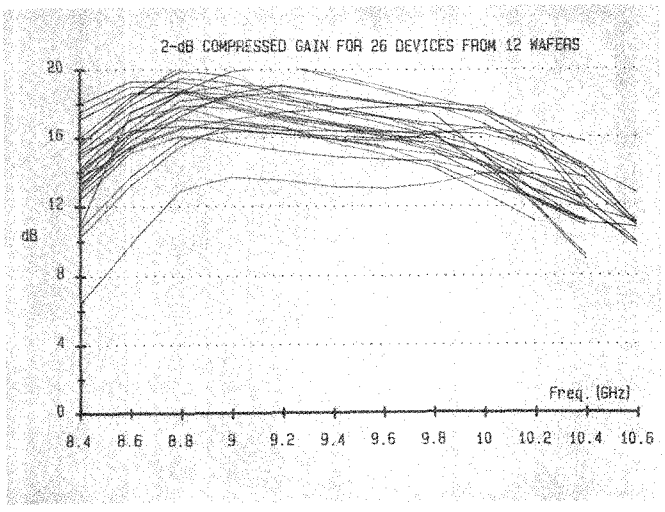


Fig. 6 2dB Compressed gain for 26 devices

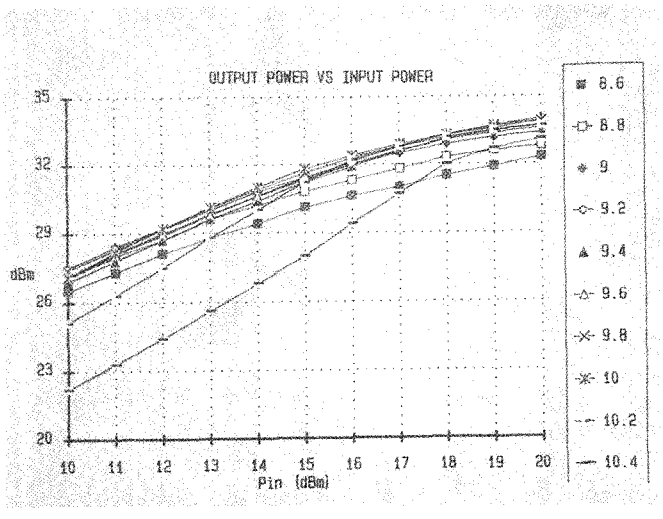


Fig. 7 Output Power vs Input Power

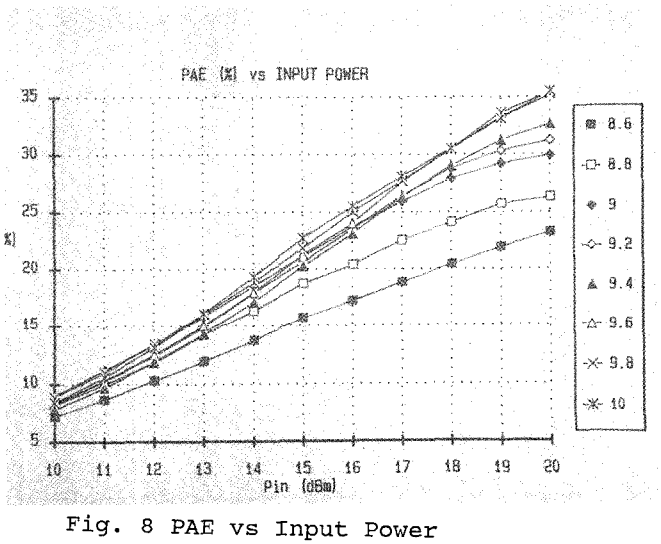


Fig. 8 PAE vs Input Power

On some wafers it was possible to operate deep in class-AB (almost class-B). Devices from 1 such wafer when biased at 9V and 7% IDSS gave a power of 33.7 dBm with 36% PAE and 10 dB gain. This clearly shows that Class-B performance is possible with a slight decrease in gain. The thermal resistance of the 2.2mm FET and the 5.76mm FET as measured by the liquid crystal technique on several die attached MMICs were 77^{o}C.mm/W and 86^{o}C.mm/W respectively, for a drain voltage of 9V, and a hot spot channel temperature of 100^{o}C.

Conclusion

A realistic solution has been successfully advanced to solve the problem of simultaneously obtaining high performance low cost X-band power amplifier modules, in large volumes. Consistent high performance with efficiencies greater than 32% at power levels of up to 2.5W over at least a 10% band have been demonstrated, using a MMIC implementation. A survey of published literature to date leads us to believe that the results shown in this paper have advanced the state-of-the-art.

References

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